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10/820,464	04/08/2004	Graeme Storm	02EDI46652637	7257

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EXAMINER	
QUIETT, CARRAMAH J	
ART UNIT	**PAPER NUMBER**
2622	

NOTIFICATION DATE	DELIVERY MODE
12/17/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/820,464	STORM ET AL.	
	Examiner	Art Unit	
	Carramah J. Quiett	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment(s), filed on 10/04/2007, have been entered and made of record. Claims 14-36 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 14-36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 14-36** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent **claims 14, 21, and 31** each recite the following limitation, "...selecting between the linear output signal and the logarithmic output signal as an output signal, with the linear output signal being selected when greater than a predetermined value." In the Remarks filed on 10/04/2007 (page 9), the Applicants stated that support for this amendment can be found in paragraph 24 of the Applicants' specification. However, the portion regarding "...the linear

output signal being selected when greater than a predetermined value" is not discussed in paragraph 24 and in other parts of the Applicants' specification. Instead, paragraph 25 of the Applicants' specification teaches that "linear values greater than A [i.e. threshold value] are taken to be saturated or near saturation, and are *replaced* by *log values* to which the offset A is added." Respectfully, for prior art examination purposes, the Examiner will *not* consider the limitation, "...the linear output signal being selected when greater than a predetermined value" in regards to claims 14, 21, and 31.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 14-36** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **Claims 14, 21, and 31** each recite the limitation "...the linear output signal being selected *when greater than a predetermined value*" in the last portion the claims (14, 21 and 31). Respectfully, please specify which type of output signal is "greater than a predetermined value" – i.e. is it the output signal, the linear output signal, and/or the logarithmic output signal? There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. **Claims 14-16, 21-26, and 31-33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al. ("CMOS Active Pixel Image Sensor with Combined Linear and Logarithmic Mode Operation"; Department of Electrical Engineering, University of Waterloo, On; 1998 IEEE Canadian Conference on Electrical and Computer Engineering; 24-28 May 1998; vol. 2; p. 754-757) – herein referred to as *Tu* in view of Serizawa et al. (U.S. Pat. #6,593,970).

For **claim 14**, Tu discloses an image sensor (fig. 1), comprising:

an array of pixels (p. 754, paragraphs 4-5), each pixel (fig. 2) comprising

a photodiode (p. 754, paragraph 5; fig. 2 a/b),

a first output circuit for deriving a linear output signal by applying a reset signal to said photodiode and reading a voltage on said photodiode after an integration time (p. 755, paragraph 3 – *Linear Integration mode*; fig. 2a), and

a second output circuit for deriving a logarithmic output signal by reading a near instantaneous illumination-dependent voltage on said photodiode that is a logarithmic function of the illumination (p. 755-756, paragraph 4 – *Logarithmic mode*, fig. 2b), and

an output selection circuit (a control signal) for selecting between the linear output signal and the logarithmic output signal as an output signal (p. 754, Abstract and paragraph 3), ~~with the linear output signal being selected when greater than a predetermined value~~ (not considered as discussed in the 112 Rejection section).

However, Tu does not expressly teach said first and second output circuits *sequentially* providing the linear and logarithmic output signals.

In a similar field of endeavor, Serizawa discloses an image sensor (fig. 1, ref. 101) that said first and second output circuits *sequentially* providing the linear and logarithmic output

signals (col. 8, lines 12-22). In light of the teaching of Serizawa, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image sensor of Tu with the image sensor as claimed in claim 14 in order to a superior method for generating a dynamic range expanded video signal (Serizawa, col. 1, lines 32-35).

For **claim 15**, Tu, as modified by Serizawa, discloses the image sensor according to claim 14, wherein said first output circuit (fig. 2a) comprises:

a reset switch (pixel reset transistor) for applying a reset voltage to said photodiode, said reset switch comprising a reset transistor including a conducting terminal connected to said photodiode (p. 754, paragraph 5); and

a readout switch (source-follower amplifier) for turning on the conducting terminal of said reset transistor after expiration of the integration time (p. 754, paragraph 5; p. 755, paragraph 4).

For **claim 16**, Tu, as modified by Serizawa, discloses the image sensor according to claim 14, wherein said second output circuit (fig. 2b) comprises:

an amplifier (source-follower amplifier; p. 754, paragraph 5); and

a log select switch for connecting said amplifier to said photodiode (p. 755, paragraph 4).

For **claim 21**, Tu discloses the image sensor (fig. 1) comprising:

an array of pixels (p. 754, paragraphs 4-5), each pixel (fig. 2)comprising

a photodiode (p. 754, paragraph 5; fig. 2 a/b),

a first output circuit connected to said photodiode for generating an output signal to be a linear output signal (p. 755, paragraph 3 – *Linear Integration mode*; fig. 2a), and

a second output circuit connected to said photodiode for generating the output signal to be a logarithmic output signal (p. 755-756, paragraph 4 – *Logarithmic mode*, fig. 2b),

an output selection circuit (a control signal) for selecting between the linear output signal and the logarithmic output signal as an output signal (p. 754, Abstract and paragraph 3), ~~with the linear output signal being selected when greater than a predetermined value~~ (not considered as discussed in the 112 Rejection section).

However, Tu does not expressly teach said first and second output circuits *sequentially* providing the linear and logarithmic output signals.

In a similar field of endeavor, Serizawa discloses an image sensor (fig. 1, ref. 101) that said first and second output circuits *sequentially* providing the linear and logarithmic output signals (col. 8, lines 12-22). In light of the teaching of Serizawa, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image sensor of Tu with the image sensor as claimed in claim 21 in order to a superior method for generating a dynamic range expanded video signal (Serizawa, col. 1, lines 32-35).

For **claim 22**, Tu, as modified by Serizawa, discloses the image sensor according to claim 21, wherein the linear output signal is selected if the pixel has not saturated during generation of the linear output signal, otherwise, the logarithmic output signal is selected (p. 755, paragraph 4; p. 756, paragraphs 1-4).

For **claim 23**, Tu, as modified by Serizawa, discloses the image sensor according to claim 21, wherein said first output circuit derives the linear output signal by applying a reset signal to said photodiode and reading a voltage on said photodiode after an integration time (p. 755, paragraph 3 – *Linear Integration mode*; fig. 2a).

For **claim 24**, Tu, as modified by Serizawa, discloses the image sensor according to claim 21, wherein said second output circuit derives a logarithmic output signal by reading a near instantaneous illumination-dependent voltage on the photodiode that is a logarithmic function of the illumination (p. 755, paragraph 4; p. 756, paragraphs 1-4).

Claims 25-26 are claims corresponding to the claims 15-16, respectively. Therefore, claims 25-26 are analyzed and rejected as previously discussed with respect to claims 15-16, respectively.

For **claim 31**, Tu teaches a method for operating an image sensor comprising an array of pixels (p. 754, paragraphs 4-5), each pixel comprising a photodiode (p. 754, paragraph 5; fig. 2 a/b), the method comprising:

deriving a linear output signal from each pixel (p. 755, paragraph 3 – *Linear Integration mode*; fig. 2a);

deriving a logarithmic output signal from each pixel with the linear and logarithmic output signals (p. 755-756, paragraph 4 – *Logarithmic mode*, fig. 2b); and

selecting between the linear output and the logarithmic output signal as an output signal (p. 754, Abstract and paragraph 3; p. 755, paragraph 4; p. 756, paragraphs 1-4), ~~with the linear output signal being selected when greater than a predetermined value~~ (not considered as discussed in the 112 Rejection section).

However, Tu does not expressly teach the image sensor with the linear and logarithmic output signals being sequentially derived.

In a similar field of endeavor, Serizawa teaches an image sensor (fig. 1, ref. 101) with the linear and logarithmic output signals being sequentially derived (col. 8, lines 12-22). In light of

the teaching of Serizawa, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of operating the image sensor of Tu with the image sensor as claimed in claim 31 in order to a superior method for generating a dynamic range expanded video signal (Serizawa, col. 1, lines 32-35).

For **claim 32**, Tu, as modified by Serizawa, teaches the method according to claim 31, wherein deriving the linear output signal from each pixel comprises:

applying a reset voltage to the photodiode (p. 754, paragraph 5);

allowing for a predetermined integration time (p. 755, paragraph 1); and

reading an output voltage on the photodiode (p. 754, paragraph 5; p. 755, paragraph 4).

For **claim 33**, Tu teaches the method according to claim 31, wherein deriving the logarithmic output signal is based upon reading a near instantaneous illumination-dependent voltage on the photodiode that is a logarithmic function of the illumination (p. 755, paragraph 4; p. 756, paragraphs 1-4).

10. **Claims 17 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tu* in view of Serizawa et al. (U.S. Pat. #6,593,970) as applied to claims 16 and 26 above, and further in view of Luo et al. (U.S. Pat. #7,071,982).

For **claim 17**, Tu, as modified by Serizawa, discloses the image sensor according to claim 16, wherein said amplifier is connected to the conducting terminal of said reset transistor. However, Tu, as modified by Serizawa, does not expressly disclose wherein said amplifier comprises a differential amplifier having an inverting input connected to the conducting terminal of said reset transistor, and a non-inverting input connected to a reference voltage.

In a similar field of endeavor, Luo discloses the image sensor (fig. 2), wherein said amplifier comprises a differential amplifier (36) having an inverting input connected to the conducting terminal of said reset transistor (V_{PH}), and a non-inverting input connected to a reference voltage (V_{REF}). Please read Luo, col. 5, lines 25-46. In light of the teaching of Luo, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the amplifier of Tu with a differential amplifier as claimed in claim 17 in order to improve the image capture efficiency thereby providing an image with increased wide dynamic range as well as improving power consumption (Luo, col. 1, line 63 – col. 2, line 39).

Claim 27 is a claim corresponding to claim 17. Therefore, claim 27 is analyzed and rejected as previously discussed with respect to claim 17.

11. **Claims 18-19, 28-29, and 34-35** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tu* in view of Serizawa et al. (U.S. Pat. #6,593,970) as applied to claims 14, 21, and 31 above, and further in view of Kusaka et al. (US 2005/0052557) – herein referred to as Kusaka.

For **claim 18**, Tu, as modified by Serizawa, discloses the image sensor according to claim 14. However, Tu, as modified by Serizawa, does not expressly teach further comprising a calibration circuit for calibrating each pixel before deriving the logarithmic output signal.

In a similar field of endeavor, Kusaka discloses an image sensor (fig. 1, ref. 1) comprising a calibration circuit (fig. 1, refs. 4-6) for calibrating each pixel before deriving the logarithmic output signal (p. 3-4, paragraphs 54-71). Also, please see Kusaka, figs. 2-3. In light of the teaching of Kusaka, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify the image sensor of Tu with a calibration circuit as claimed in claim 18 in order to automatically achieve an improved wide brightness range as well as an improved a narrow brightness range (p. 1, paragraphs 7-12).

For **claim 19**, Tu, as modified by Serizawa and Kusaka, discloses the image sensor according to claim 18, wherein said calibrating circuit comprises a constant current source selectively connected to each respective pixel (p. 3, paragraph 60; fig. 3).

Claims 28-29 are claims corresponding to the claims 18-19, respectively. Therefore, claims 28-29 are analyzed and rejected as previously discussed with respect to claims 18-19, respectively.

Claims 34-35 are claims corresponding to the claims 18-19, respectively. Therefore, claims 34-35 are analyzed and rejected as previously discussed with respect to claims 18-19, respectively.

12. **Claims 20, 30, and 36** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tu* in view of Serizawa et al. (U.S. Pat. #6,593,970) as applied to claims 19, 29, and 35 above, and further in view of He et al. (US 6,355,965) – herein referred to as He.

For **claim 20**, Tu, as modified by Serizawa and Kusaka (fig. 3) discloses the image sensor according to claim 19, wherein an output node (Kusaka fig. 3, the node between T1 and T2) is associated with each photodiode, and wherein the linear and logarithmic output signals are derived from the output node (Kusaka, p. 3-4, paragraphs 63-64). However, Tu, as modified by Serizawa and Kusaka, do not expressly disclose said calibration circuit further comprising a switch connected between said photodiode and the output node for isolating said photodiode from the output node while calibration takes place.

In a similar field of endeavor, He discloses a calibration circuit comprising a switch (fig. 4, S2) connected between said photodiode and the output node for isolating said photodiode from the output node while calibration takes place (col. 4, lines4-23). In light of the teaching of He, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image sensor of Tu, as modified by Kusaka, with a switch as claimed in claim 20 in order to change to calibration mode (He, col. 4, lines4-23).

Both of **claims 30 and 36** are claims corresponding to the claim 20. Therefore, claims 30 and 36 are each analyzed and rejected as previously discussed with respect to claim 20.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571) 272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CJQ
December 10, 2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER